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Director, EPTAC



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IPC-6012

**A Review, What is it?
and
Who Uses it?**



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IPC-6012

Title:

Qualification and Performance Specification for Rigid Printed Boards



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Scope

The document establishes and defines the qualification and performance requirements for the fabrication of rigid printed boards.



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Purpose

Provides information on following Technologies:

- **Single sided and double sided with and without plated through holes**
- **Multilayer boards with PTH, with and without buried/blind vias**
- **Multilayer boards containing High Density Interconnect (HDI)**
- **Active embedded passive circuitry printed boards.**
- **Metal core board.**



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How is it used?

- This document is a derivative document.
 - To meet the IPC requirements, the following issues need to be addressed.
 - Design Criteria, based upon the 2200 series documents.
 - Laminate selection based upon the 4101 document.
 - This continues from board fabrication through manufacturing and shipping to the customer.



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How is it used?

- This document is used:
 - By the board shops to manufacture the raw boards.
 - to qualify and inspect the raw boards coming from the board shops
 - to define the AQL for inspection of incoming boards.
- This document also defines the test coupons to be used to evaluate different characteristics of the raw board.



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How is it used?

- This document list 26 different test from IPC-TM-650 to evaluate the product.
- It also lists all the IPC document from the design requirements, to adhesives, base materials, solder mask, testing procedures etc.



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How is it used?

- It defines the different plating requirements for the various class of products being manufactured, as shown in Table 3-3



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Table 3-3

Table 3-3 Surface and Hole Copper Plating Requirements for Through-Holes, Blind, and Buried Vias > 2 Layers¹

	Class 1	Class 2	Class 3
Copper – average ²	20 µm [787 µin]	20 µm [787 µin]	25 µm [984 µin]
Minimum thin areas ³	18 µm [709 µin]	18 µm [709 µin]	20 µm [787 µin]
Minimum Wrap ⁴	AABUS	5 µm [197 µin]	12 µm [472 µin]

Note 1. Does not apply to microvias. Blind vias have greater than 1:1 aspect ratio.

Note 2. Copper plating (1.3.4.2) thickness **shall** be continuous and wrap from hole walls onto outer surfaces. Refer to IPC-A-600 for discussion on copper plating thickness for hole walls.

Note 3. For Class 3 PBs having a drilled hole diameter ≤ 0.35 mm [0.0138 in] and having an aspect ratio > 3.5:1, the minimum thin area copper plating in the hole **shall** be 25 µm [984 µin].

Note 4. Wrap copper plating for filled PTHs and vias **shall** be in accordance with 3.6.2.11.1.



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How is it used?

- The type of coating to be used has to be defined in the contract between the manufacturer and the user as it is inspected to the requirement of this document
- The final finishes and coating requirements are defined in this document.



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Table on Finishes

Table 3-2 Final Finish and Coating Requirements

Code	Finish	Thickness	Applicable Acceptability Specification	Marking Code ¹
S	Solder Coating over Bare Copper	Coverage & Solderable ²	J-STD-006	b0
b1	Lead-Free Solder Coating over Bare Copper	Coverage & Solderable ²	J-STD-006	b1
T	Electrodeposited Tin-Lead (fused) - minimum	Coverage & Solderable ²	J-STD-006	b3
X	Either Type S or T	As indicated by code		
TLU	Electrodeposited Tin-Lead Unfused - minimum	8.0 µm [315 µin]	J-STD-006	b3
G	Gold for edge-board connectors and areas not to be soldered - minimum	Class 1 and Class 2 0.8 µm [31.5 µin]	None	b4
		Class 3 1.25 µm [49.21 µin]		
GS	Gold Electroplate on areas to be soldered - maximum ³	0.45 µm [17.72 µin]	None	b4
GWB-1	Gold Electroplate for areas to be wire bonded (ultrasonic) - minimum	0.05 µm [1.97 µin]	None	b4
	Electrolytic nickel under gold for areas to be wire bonded (ultrasonic) - minimum	3 µm [118 µin]	None	b4



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Section 3.3 Visual

This section covers visual examination of the printed board such as:

- Edges
- Laminate imperfections
- Measling
- Crazing
- Delamination/blistering
- Foreign inclusions
- Weave exposure
- Bow and Twist
- etc



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3.4 Printed Board Dimensional Requirements

Internal Inspection of:

- Hole Size
- Pattern Accuracy and Pattern Feature Accuracy
- Annular Ring Breakout, internal and external



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3.5 Conductor Definition

- Discusses:
 - Width and Thickness
 - Spacing
 - Imperfections
 - Nick and pinholes
 - SMT land
 - Wire bond pads
 - Edge connector lands
 - Dewetting/nonwetting
 - Final finish



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3.6 Structural Integrity

Discusses structural integrity for thermally stress evaluation of test coupons defined in 3.6.2

- Plating integrity and voids
- Laminate voids and cracks
- Delamination
- Etchback
- Smear removal
- Hole breakout, internal and external
- Lifted lands
- Plating thickness
- Foil thickness, internal and external
- Metal cores



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Table 3-6 Plated Hole Integrity After Stress

Property	Class 1	Class 2	Class 3
Copper voids	Three voids allowed per hole. Voids in the same plane are not allowed. No void shall be longer than 5% of board thickness. No circumferential voids greater than 90° allowed.	One void allowed per specimen provided the additional microsection criteria of 3.6.2.2 are met.	One void allowed per specimen provided the additional microsection criteria of 3.6.2.2 are met.
Plating folds/inclusions	The minimum copper thickness in Table 3-2 must be met. For positive etchback, measurements should follow the topography of the dielectric. When negative etchback results in folds in the copper plating, the copper thickness shall meet the minimum requirements as measured from the face of the internal layer; negative etchback limits shall not be exceeded. See Figure 3-11. Sample must be microetched to evaluate.		
Burrs and nodules ⁴	Allowed if minimum hole diameter is met.	Allowed if minimum hole diameter is met.	Allowed if minimum hole diameter is met.
Glass fiber protrusion	Allowed. See 3.6.2.11.	Allowed. See 3.6.2.11.	Allowed. See 3.6.2.11.
Wicking (Copper Plating)	125 µm [4,921 µin] maximum	100 µm [3,937 µin] maximum	80 µm [3,150 µin] maximum
Innerlayer inclusions (inclusions at the interface between internal lands and through hole plating)	Allowed on only one side of hole wall at each land location on 20% of each available land.	None allowed.	None allowed.
Internal foil cracks ¹	"C" cracks allowed on only one side of hole provided it does not extend through foil thickness.	None allowed.	None allowed.
External foil cracks ¹ (Type "A," "B" and "D" cracks)	"D" cracks not allowed. "A" and "B" cracks allowed.	"D" and "B" cracks not allowed. "A" cracks allowed.	"D" and "B" cracks not allowed. "A" cracks allowed.
Barrel/Corner cracks ¹ (type "E" and "F" cracks)	None allowed.	None allowed.	None allowed.



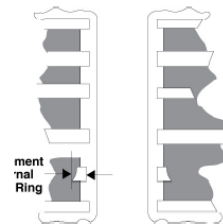
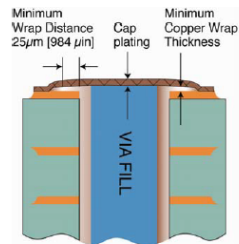
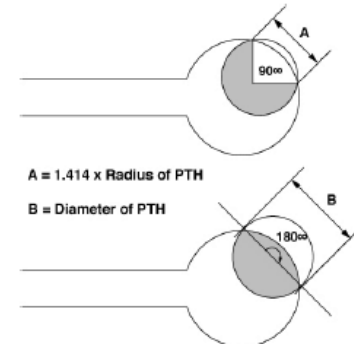
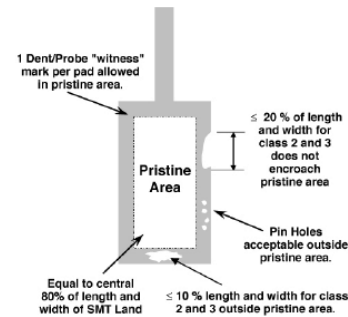
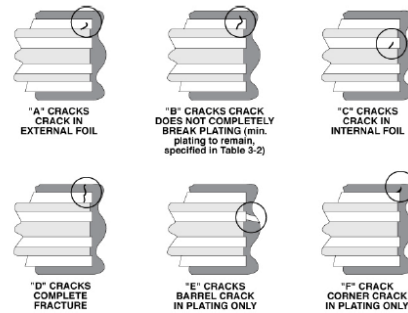
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Illustrations



Note: Cap plating, if required, over filled holes is not considered in wrap copper thickness measurements.
Figure 3-16 Surface Copper Wrap Measurement (Applicable to all filled PTHs)

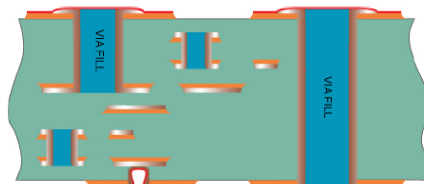


Figure 3-17 Wrap Copper in Type 4 PB (Acceptable)



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3.7 Solder Mask

- Solder mask coverage, cure, adhesion, thickness, etc.

Table 3-10 Solder Mask Adhesion

Surface	Maximum Percentage Loss Allowed		
	Class 1	Class 2	Class 3
Bare Copper	10	5	0
Gold or Nickel	25	10	5
Base Laminate	10	5	0
Melting Metals (Tin-lead plating, fused tin-lead, and bright acid-tin)	50	25	10



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3.8 Through 3.10

- 3.8 Electrical Requirements
- 3.9 Cleanliness
- 3.10 Special Requirements
- 3.11 Repair
- 3.12 Rework



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4.0 Quality Assurance Provisions

This section address

- Qualification testing
- Acceptance testing



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Test Table

PB Type: PBs without PTHs (Type 1) and with PTHs (Types 2-6) are classified as follows:

Type 1—Single-Sided PB

Type 2—Double-Sided PB

Type 3—Multilayer PB without blind or buried vias

Type 4—Multilayer PB with blind and/or buried vias

Type 5—Multilayer metal core PB without blind or buried vias

Type 6—Multilayer metal core PB with blind and/or buried vias

Table 4-1 Qualification Test Coupons

Test	Type 1	Types 2,3,5	Types 4, 6	PB ³
Visual ¹	All	All	All	X
Solderability Surface ¹ Hole ¹	M2, M5	S1,S6	S1,S6	
Dimensional ¹	All	All	All	X
Physical Plating Adhesion ¹ Bond Strength	N1, N4, N5 A2, A3, A6	N1, N4, N5	N1, N4, N5	
Construction Integrity PTH Prior to Stress Additional Dimensions		A1, A4, A5 A1, A4, A5	Design Req. Design Req.	
PTH After Stress Thermal Stress Horizontal micro (Metal Core) Rework Simulation		A1, A4, A5 B4, B5 B3, B6	Design Req. A1, B4, B5 Design Req.	



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From 2221 12.4.7 Coupon M

- **(Surface Mount Solderability - Optional)** The coupon shall be as shown in Figure 12-18.
- This coupon may be used to evaluate solderability of surface mount lands to IPC-J-STD-003 requirements. If it is used, the test method and performance criteria shall be specified in the procurement documentation.

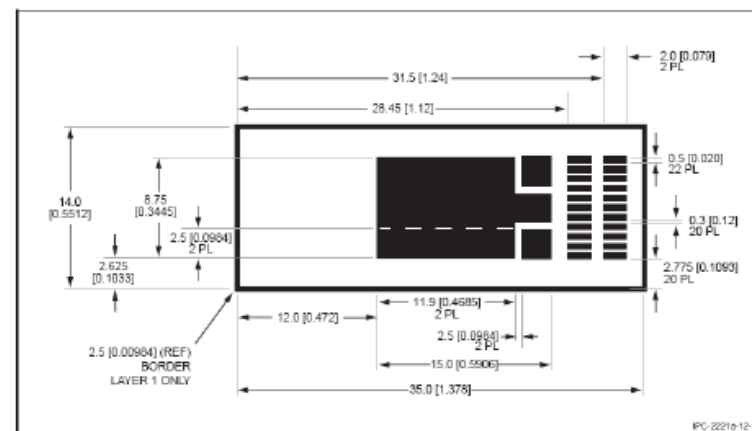


Figure 12-18 Test Coupon M. Surface Mounting Solderability Testing, mm [in]



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From 2221 12.4.8 Coupon N

(Peel Strength, Surface Mount Bond Strength - Optional for SMT) This coupon shall be as shown in Figure 12-19. Coupon N is used for evaluating peel strength and may be used to evaluate the bond strength of surface mount lands. If it is used, the test method and performance criteria shall be specified in the procurement documentation.

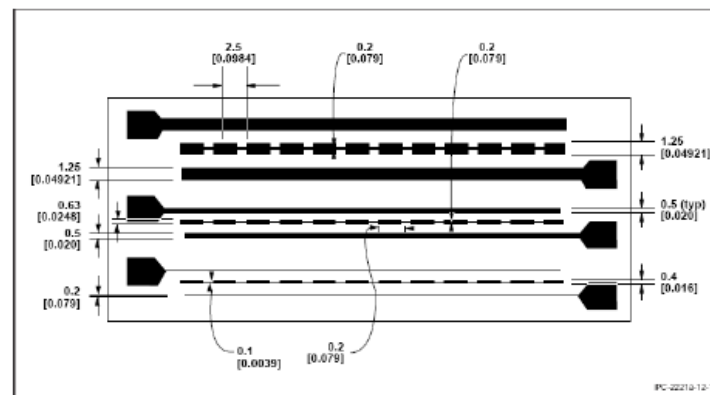


Figure 12-19 Test Coupon N, Surface Mounting Bond Strength and Peel Strength, mm [in]



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Thank You
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Further Information

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Leo Lambert at leo@eptac.com or call at
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